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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,452	01/23/2004	Robert L. Terry	AE-28 / TEC1286-01	2037

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EXAMINER	
RO, BENTSU	

ART UNIT	PAPER NUMBER
2837	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,452	TERRY ET AL.	
	Examiner	Art Unit	
	Bentsu Ro	2837	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-39 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 33-35 is/are allowed.

6)☒ Claim(s) 1,2,9,14-19,21,22,25,26,29,30 and 36-39 is/are rejected.

7)☒ Claim(s) 3-8,10-13,20,23,24,27,28,31 and 32 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date various dates. (4 sheets)
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FIRST OFFICE ACTION

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 25, 26, 29, 30 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Erdman US Patent No. 5,376,866.

Claims read onto Erdman's teaching as follows:

The claims:	**Erdman's teaching:**
25. A method for detecting a locked or stopped rotor in a motor control system	Erdman teaches a method (and an apparatus) for detecting a motor running underspeed in a motor control system, see Fig. 25a-25b, the operational amplifiers 414, 416, 418, 420; it is noted that underspeed includes a "lock" or a "stop" of the rotor; it is further noted that, even though Erdman calls the circuit as "underspeed detector circuit", the circuit itself is also capable to detect a locked or a stopped rotor;
for a brushless and sensorless DC motor system	the Erdman's motor system is a brushless motor, see column 2, line 13, the words "brushless motors", for example; further, Erdman teaches the commutation method for the brushless motor using a sensor (see Fig. 6) or without using a sensor (see Fig. 16);

having a plurality of phase coils driven by power drivers,	Fig. 6 shows windings 22a-22d, the windings are driven by Darlington transistors 82a-d and 83a-d; thus, the Darlington transistors 82a-d and 83a-d are power drivers; Fig. 25b at the right-hand side, it shows four leads 384, 386, 388, 390, these leads are connector terminals for connecting to the motor windings; Fig. 25b also shows power transistors 362-364 as "power drivers";
comprising the steps of:	
disabling the power drivers;	Fig. 25b shows a transistor 422 for disabling the power transistors 362-364; see column 24, lines 37-42;
then measuring the back EMF generated from the plurality of phase coils;	Fig. 25a, at the very left, there are four terminals 384-390, these four terminals are the same terminals as shown in Fig. 25b, at the right-hand side; the terminals 384-390 (Fig. 25a) are connected to an operational amplifier 382 for measuring the back EMF generated by the motor windings;
then enabling the power drivers after a time period dependent on the measured back EMF.	as long as the motor is stopped, locked or underspeed, the transistor 422 will be OFF to disconnect the power transistors 362, 364; however, after a certain period of time, when the motor is running at a normal speed, the power transistors 362-364 will be ON again; this "certain period of time" depends on the measured back EMF, measured by the operational amplifier 382 (Fig. 25a).
26. The method of claim 25, further comprising steps after the step of then measuring the back EMF:	

if measured back EMF is above a preset threshold, setting the time period to zero.	Fig. 25a, at the non-inverting input of operational amplifier 382, there is a resistor 598 connected thereto, this resistor 598 provides a preset threshold; column 24, line 20 describes "...when this integrated voltage reaches a reference level...", this "reference level" is a preset threshold; as soon as this preset threshold is reached, the motor resumes to a normal operational condition; thus, there is no delay, and the time period is zero.
29. The method of claim 25, further comprising the steps of: measuring a motor supply voltage; and upon the measured voltage being above or below a preset range, disabling the power drivers.	 Fig. 25a shows an over or under voltage detection circuit, this over/under voltage detection circuit includes operational amplifiers 410 and 412, and various divider resistors for measuring a motor supply voltage; the op amps 410 and 412 control the transistor 422 to either enable or disable the power transistors 362, 364, depending the measured voltage is over/under or normal; see column 24, lines 33-42.
30. The method of claim 25, further comprising the steps of: measuring a motor supply current supplied to at least one of the plurality of phase coils, and upon the measured current being above or	 Fig. 19 shows a current sensing circuit for measuring the current of at least one motor winding; the Fig. 19 circuit includes a current sensing resistor 204, connected in series with a motor winding; the "INHIBIT" terminal shown at the right-

below a preset range, disabling the power drivers to the plurality of phase coils.	hand side of Fig. 19 is to disable the power transistors; see column 16, lines 24-37.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 9, 14-19, 21, 22, 36-39 are all rejected under 35 U.S.C. 103(a) as being unpatentable over Erdman.

Claims read onto Erdman's teaching as follows:

1. A motor control system for controlling a brushless and sensorless DC motor system having a plurality of phase coils, comprising:	same as that of claim 25 explained previously in paragraph 2;
a motor control integrated circuit	Erdman teaches a motor control circuit, Erdman does not teach "integrated" circuit; however, in nowadays technology, the "integrated circuit" is commonly used and is desirable, see more explanation at the end of this comparison chart;
having a plurality of motor driver outputs	Fig. 25b shows four motor leads 384-390 which are motor driver outputs;
and a control input for operating said plurality of output drivers,	the base terminal of transistor 422 (Fig. 25b) is a control input;
said plurality of motor driver outputs coupled to the plurality of phase coils; and	the motor leads 384-390 are connected to the motor windings (not shown in Fig. 25b but clearly shown in Fig. 6);

a fault detection circuit	Fig. 25a, the over/under voltage detection circuit (op amps 410 and 412) and under speed detection circuit (op amps 414-420), and the associated circuit elements, such as op amp 382, NAND gates 446, 448, etc together constitute a fault detection circuit;
coupled with said control input and capable of selectively switching the state of ***said control signal (this phase lacks antecedent basis)*** to momentarily disable said plurality of output drivers,	op amps 410, 412, 420 all connect to the base of transistor 422; the transistor 422 controls the enable/disable of power transistors 362, 364, see column 24, lines 33-42;
said fault detection circuit being coupled to at least one of the plurality of phase coils	all circuit elements are coupled together, including the op amps coupled to the motor windings, see Figs. 25a-25b;
and is capable of detecting a threshold back EMF voltage from the at least one of the plurality of phase coils.	the op amp 382 acts as an integrator to detect the back EMF of the windings; the back EMF is compared with a reference level, which reference level is a threshold; see column 24, line 20.
2. The motor control system of claim 1, wherein said fault detection circuit includes a capacitor coupled to the at least one of the plurality of phase coils,	Fig. 25a, in the op amp 382, there is a passive capacitor 460 connected to the op amp 382 such that the op amp 382 functioned as an integrator; it is noted that the capacitor 460 is connected to the terminals 386 via an electronic switch 392; the terminal 386 is a motor winding lead;
said capacitor receiving back EMF	the capacitor 460 and the op amp 382 integrate the back EMF of the motor windings;
and said fault detection circuit detecting said threshold back EMF voltage across said capacitor.	the voltage across the capacitor 460 provides a feedback signal to op amp 382 so that the op amp 382 can be either in a HI state or in a Low state based on the integrated back EMF value.

9. All same as claim 1 except the "electrical and nonelectrical fault conditions of the motor system".	op amps 410, 412 constitute part of the over/under voltage detection circuit for detecting an over or under voltage of the motor system, which over/under voltage is an electrical fault condition; op amps 414-420 constitute part of the udnerspeed detector circuit, which is a non electrical fault.
14. The motor control system of claim 9, further comprising a voltage sensing circuit coupled to a voltage supply of the system, said voltage sensing circuit coupled to said fault detection circuit, said fault detection circuit capable of switching said control input to disable said plurality of motor driver outputs upon said voltage supply being above or below a preset limit.	Fig. 25a shows a voltage divider circuit having resistors 620, 622, 624; the voltage divider circuit is a voltage sensing circuit; the voltage divider circuit is connected to the op amps 410 and 412; the outputs of op amps 410, 412 are connected to the base of transistor 422; transistor 422 controls the enable/disable of the power transistors 362, 364; see column 24, lines 35-42.
15.	similar to that of claim 30; see Fig. 19.
16. The motor control system of claim 9, wherein said motor control integrated circuit outputs a speed signal related to motor speed, ...	the voltage across the capacitor 506 (Fig. 25b, at the lower-left corner) represents a motor speed signal, see column 26, lines 42-44; the remaining of claim 16 is similar to previous explanation.
17. The motor control system of claim 9, wherein said control input is an over current protection input of said motor control integrated circuit.	based on the examiner's understanding, the "INHIBIT" terminal of Fig. 19 should connect to the base of transistor 422 of Fig. 25b.
18, 19, 21, 22, 36, 37, 39.	the subject matter of these claims has been explained previously, further discussion is deemed un-necessary.

38. The actuator control system of claim 37, wherein said voltage measuring circuit includes a microcontroller.	the op amps 410 and 412 can be constructed in a form of microcontroller.

With respect to the claims, Erdman teaches each and every item as shown in the above comparison chart except "integrated" circuit. In nowadays technology, a great portion of the control circuits is designed in integrated form for a specific function or for a specific application. These types of integrated circuits are known as "Application Specific Integrated Circuits", or "ASICs".

Then why using an ASIC?? An ASIC is an integrated circuit having the same circuit components and circuit function as the "discrete component" and "hardwired" control circuit. Using ASIC simplifies the assembling step and therefore lowers the manufacturing cost. Because ASIC has these advantages, there is a trend for using ASIC in most control circuits.

5. Claim 1, line 7, the recitation "said control signal" lacks antecedent basis. The examiner has not checked the proper antecedent of all claimed elements. It is applicant's responsibility to do so.

6. Claims 3-8, 10-13, 20, 23, 24, 27, 28, 31, 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 33-35 are allowable.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any inquiry concerning this communication should be directed to Bentsu Ro at telephone number (571) 272-2072.

2/3/2005

Bentsu Ro
Senior Examiner
Art Unit 2837